

CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

- 1 1. An analog front end system, comprising:
 - 2 a digital-to-analog converter;
 - 3 a line driver, electrically coupled to said digital-to-analog converter;
 - 4 a hybrid, electrically coupled to said line driver;
 - 5 a multiple-input device having a plurality of inputs and at least one output,
 - 6 wherein at least one of said inputs is electrically coupled to said hybrid;
 - 7 an analog-to-digital converter, electrically coupled to said output of said multiple-
 - 8 input device;
 - 9 an isolation circuit configured to maintain direct-current isolation between the
 - 10 terminals of said isolation circuit, wherein:
 - 11 said isolation circuit is electrically coupled to at least one of said inputs of
 - 12 said multiple-input device; and
 - 13 said isolation circuit comprises a plurality of resistance elements and a
 - 14 plurality of capacitance elements, electrically coupled;
 - 15 a ground circuit configured to provide a ground reference, wherein:
 - 16 said ground circuit is electrically coupled to at least one of said inputs of
 - 17 said multiple-input device; and
 - 18 said ground circuit comprises a plurality of resistance elements and at least
 - 19 one ground reference point, electrically coupled; and

20 a processing circuitry, said processing circuitry being configured to control said
21 digital-to-analog converter, said line driver, said analog-to-digital converter, and said
22 multiple-input device in response to commands received by said processing circuitry.

1 2. The analog front end system of claim 1, wherein said multiple-input
2 device is configured such that said inputs are selectively operational.

1 3. The analog front end system of claim 1, wherein said multiple-input
2 device is a multiplexer.

1 4. An analog front end system, comprising:
2 a digital-to-analog converter;
3 a line driver, electrically coupled to said digital-to-analog converter;
4 means for multiplexing a plurality of inputs to at least one output, electrically
5 coupled to said line driver; and
6 an analog-to-digital converter, electrically coupled to said means for multiplexing.

1 5. The analog front end system of claim 4, further comprising a hybrid,
2 electrically coupled between said line driver and one of said inputs of said means for
3 multiplexing.

1 6. The analog front end system of claim 4, further comprising means for
2 direct current isolation of said multiple-input device from an input terminal, electrically
3 coupled to one of said inputs of said means for multiplexing.

1 7. The analog front end system of claim 4, further comprising means for
2 providing a ground reference, electrically coupled to one of said inputs of said means for
3 multiplexing.

1 8. The analog front end system of claim 4, further comprising means for
2 controlling said digital-to-analog converter, said line driver, said analog-to-digital
3 converter, and said multiple-input device responsive to commands received by said
4 means for controlling.

1 9. An analog front end system, comprising:
2 a digital-to-analog converter;
3 a line driver, electrically coupled to said digital-to-analog converter;
4 a multiple-input device having a plurality of inputs and at least one output,
5 electrically coupled to said line driver; and
6 an analog-to-digital converter, electrically coupled to said multiple-input device.

1 10. The analog front end system of claim 9, further comprising a hybrid,
2 electrically coupled between said line driver and said multiple-input device.

1 11. The analog front end system of claim 9, further comprising an isolation
2 circuit, electrically coupled to said multiple-input device.

1 12. The analog front end system of claim 11, wherein said isolation circuit
2 comprises a plurality of resistance elements and a plurality of capacitance elements,
3 electrically coupled.

1 13. The analog front end system of claim 9, further comprising a ground
2 circuit configured to provide a ground reference, electrically coupled to said multiple-
3 input device.

1 14. The analog front end system of claim 13, wherein said ground circuit
2 comprises a plurality of resistance elements and at least one ground reference point,
3 electrically coupled.

1 15. The analog front end of claim 9, wherein said multiple-input device is
2 configured such that said inputs are selectively operational.

1 16. The analog front end system of claim 9, further comprising a processing
2 circuitry, said processing circuitry being configured to control said digital-to-analog
3 converter, said line driver, said analog-to-digital converter, and said multiple-input device
4 in response to commands received by said processing circuitry.

1 17. A method for testing a DSL line, comprising the steps of:
 2 transmitting test samples to an analog front end;
 3 interpreting said test samples as multi-bit digitized values using said analog
 4 front end;
 5 generating test patterns, from said digitized values, having a plurality of
 6 samples; and
 7 testing a DSL line using said test patterns.

1 18. The method of claim 17, wherein said interpreting step comprises
 2 interpreting said test samples as 8-bit digitized values using said analog front end.

1 19. The method of claim 17, wherein said interpreting step, said generating
 2 step, and said testing step are controlled by a processing circuitry responsive to received
 3 commands.

1 20. A method for DSL line testing, comprising the steps of:
 2 providing test stimuli to a DSL line using an analog front end; and
 3 receiving responses to said test stimuli from said DSL line using said analog
 4 front end.

1 21. The method of claim 20, wherein said providing step comprises providing
 2 test stimuli to a DSL line using a digital-to-analog converter and an analog-to-digital
 3 converter of said analog front end.

1 22. The method of claim 20, wherein said providing step comprises
2 transmitting test stimuli to a DSL line on a carrier signal using an analog front end.

1 23. The method of claim 20, wherein said receiving step further comprises
2 storing said responses to said test stimuli to a computer.

1 24. A DSL line testing format, comprising:
2 a plurality of test frames, wherein:
3 said test frames comprise a plurality of multi-bit test samples; and
4 the first of said samples of said test frames comprises a test header.

1 25. The testing format of claim 24, wherein said test header comprises a test
2 control header format.

1 26. The testing format of claim 24, wherein said test header comprises a test
2 status header format.

1 27. A test header, comprising:
2 a multi-bit test control header format, said test control header format comprising:
3 a pattern length field configured to control the generation of a plurality of
4 test patterns by an analog front end;

5 a sample rate field configured to control the selection of sample rates of a
6 digital-to-analog converter and of an analog-to-digital converter;

7 a spare field, capable of being configured to control at least one function
8 of an analog front end;

9 a loop-back field configured to control a loop-back function of an analog
10 front end;

11 a hybrid field configured to control the operating status of a hybrid of an
12 analog front end; and

13 an input select field configured to control the selection of a plurality of test
14 inputs to an analog front end.

1 28. The test header of claim 27, wherein said test control header format is
2 12-bits long.

1 29. The test header of claim 28, wherein:

2 said pattern length field is 4-bits long;

3 said sample rate field is 2-bits long;

4 said spare field is 2-bits long;

5 said loop-back field is 1-bit long;

6 said hybrid field is 1-bit long; and

7 said input select field is 2-bits long.

1 30. The test header of claim 27, further comprising a buffer configured to store
2 test samples.

1 31. A test header, comprising:
2 a multi-bit test status header format, said test status header format comprising:
3 a pattern length field configured to provide identification of one or more of
4 a plurality of test patterns generated by an analog front end;
5 a sample rate field configured to provide the selection status of sample
6 rates of a digital-to-analog converter and of an analog-to-digital converter;
7 a spare field, capable of being configured to provide the status of at least
8 one function of an analog front end;
9 a loop-back field configured to provide the status of a loop-back function
10 of an analog front end;
11 a hybrid field configured to provide the operating status of a hybrid of an
12 analog front end; and
13 an input select field configured to provide the selection status of a plurality
14 of test inputs to an analog front end.

1 32. The test header of claim 31, wherein said test status header format is
2 12-bits long.

1 33. The test header of claim 32, wherein:
2 said pattern length field is 4-bits long;

- 3 said sample rate field is 2-bits long;
- 4 said spare field is 2-bits long;
- 5 said loop-back field is 1-bit long;
- 6 said hybrid field is 1-bit long; and
- 7 said input select field is 2-bits long.

- 1 34. The test header of claim 31, further comprising a buffer configured to store
- 2 test samples.

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